



# PCA9555

## 16-bit I<sup>2</sup>C-bus and SMBus I/O port with interrupt

Rev. 10 — 8 November 2017

Product data sheet

## 1. General description

The PCA9555 is a 24-pin CMOS device that provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I<sup>2</sup>C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I<sup>2</sup>C-bus I/O expanders. The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PCA9555 consists of two 8-bit Configuration (Input or Output selection); Input, Output and Polarity Inversion (active HIGH or active LOW operation) registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master. Although pin-to-pin and I<sup>2</sup>C-bus address compatible with the PCF8575, software changes are required due to the enhancements, and are discussed in *Application Note AN469*.

The PCA9555 open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I<sup>2</sup>C-bus address and allow up to eight devices to share the same I<sup>2</sup>C-bus/SMBus. The fixed I<sup>2</sup>C-bus address of the PCA9555 is the same as the PCA9554, allowing up to eight of these devices in any combination to share the same I<sup>2</sup>C-bus/SMBus.

## 2. Features and benefits

- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 16 I/O pins which default to 16 inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101



- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Five packages offered: SO24, SSOP24, TSSOP24, HVQFN24 and HWQFN24

### 3. Ordering information

Table 1. Ordering information

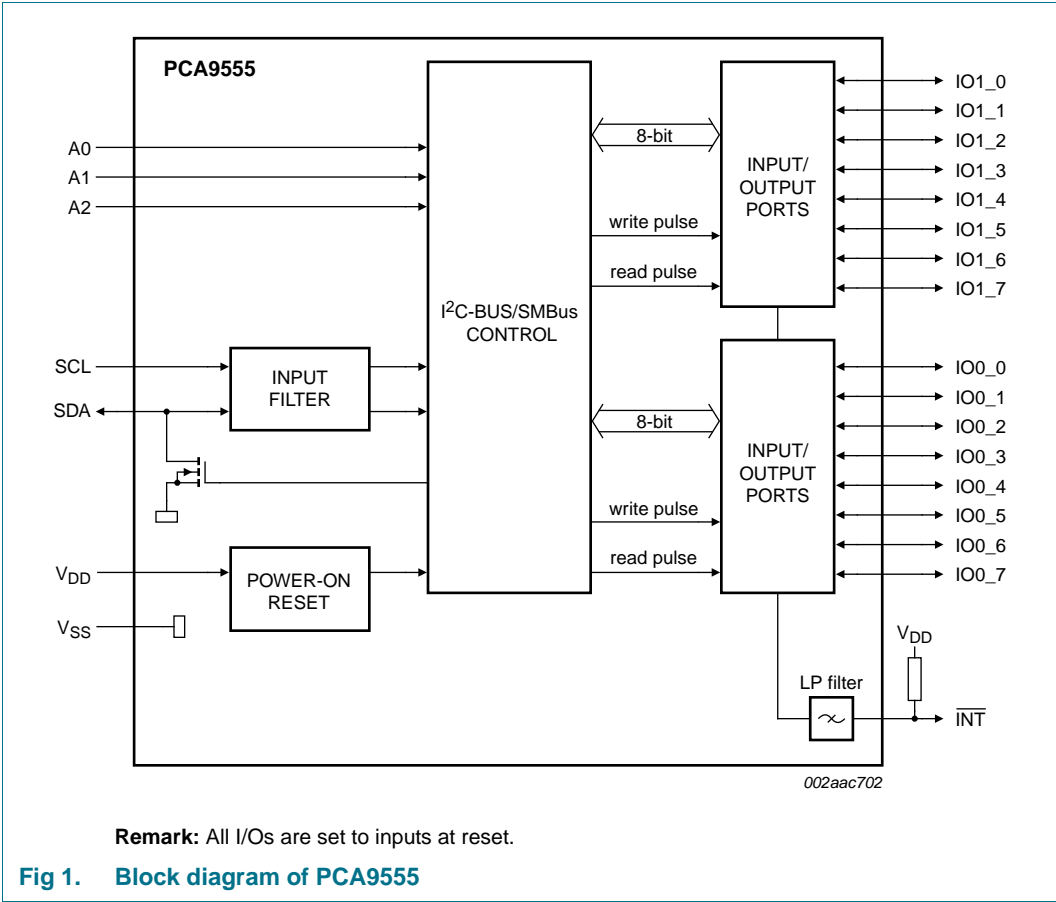
| Type number | Topside mark | Package |   |          |
|-------------|--------------|---------|---|----------|
|             |              | Name    | Description   | Version  |
| PCA9555D    | PCA9555D     | SO24    | plastic small outline package; 24 leads; body width 7.5 mm  | SOT137-1 |
| PCA9555DB   | PCA9555      | SSOP24  | plastic shrink small outline package; 24 leads; bodywidth 5.3 mm  | SOT340-1 |
| PCA9555PW   | PCA9555      | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm                                  | SOT355-1 |
| PCA9555BS   | 9555         | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm      | SOT616-1 |
| PCA9555HF   | P55H         | HWQFN24 | plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.75 mm | SOT994-1 |

#### 3.1 Ordering options

Table 2. Ordering options

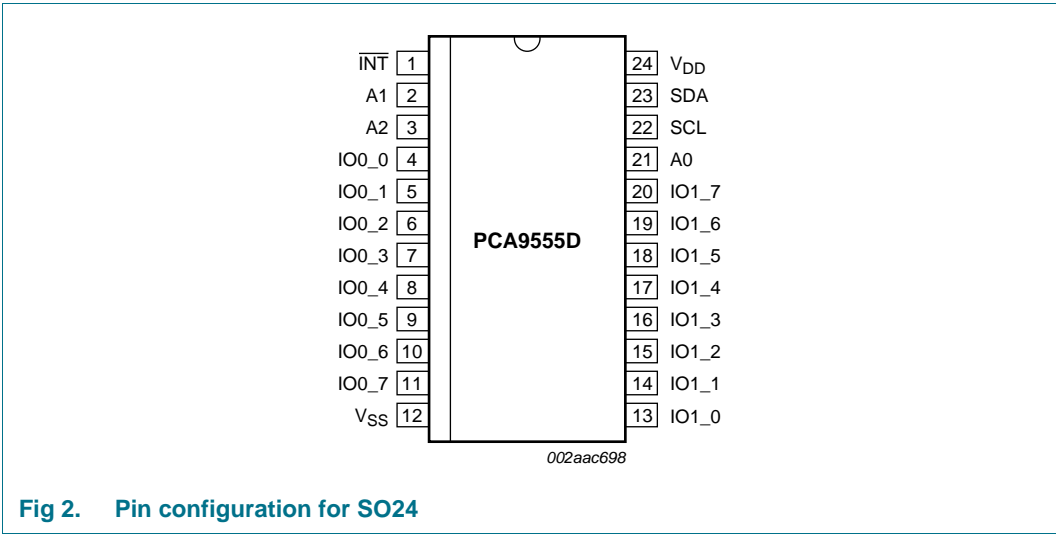
| Type number | Orderable part number | Package | Packing method                               | Minimum order quantity | Temperature                         |
|-------------|-----------------------|---------|--|------------------------|-------------------------------------|
| PCA9555D    | PCA9555D,112          | SO24    | STANDARD MARKING * IC'S TUBE - DSC BULK PACK | 1200                   | T <sub>amb</sub> = -40 °C to +85 °C |
|             | PCA9555D,118          | SO24    | REEL 13" Q1/T1 *STANDARD MARK SMD            | 1000                   |                                     |
| PCA9555DB   | PCA9555DB,112         | SSOP24  | STANDARD MARKING * IC'S TUBE - DSC BULK PACK | 826                    | T <sub>amb</sub> = -40 °C to +85 °C |
|             | PCA9555DB,118         | SSOP24  | REEL 13" Q1/T1 *STANDARD MARK SMD            | 1000                   |                                     |
| PCA9555PW   | PCA9555PW,112         | TSSOP24 | STANDARD MARKING * IC'S TUBE - DSC BULK PACK | 1575                   | T <sub>amb</sub> = -40 °C to +85 °C |
|             | PCA9555PW,118         | TSSOP24 | REEL 13" Q1/T1 *STANDARD MARK SMD            | 2500                   |                                     |
| PCA9555BS   | PCA9555BS,118         | HVQFN24 | REEL 13" Q1/T1 *STANDARD MARK SMD            | 6000                   | T <sub>amb</sub> = -40 °C to +85 °C |
|             | PCA9555BSHP           | HVQFN24 | REEL 13" Q2/T3 *STANDARD MARK SMD            | 6000                   |                                     |
| PCA9555HF   | PCA9555HF,118         | HWQFN24 | REEL 13" Q1/T1 *STANDARD MARK SMD            | 6000                   | T <sub>amb</sub> = -40 °C to +85 °C |

4. Block diagram



5. Pinning information

5.1 Pinning



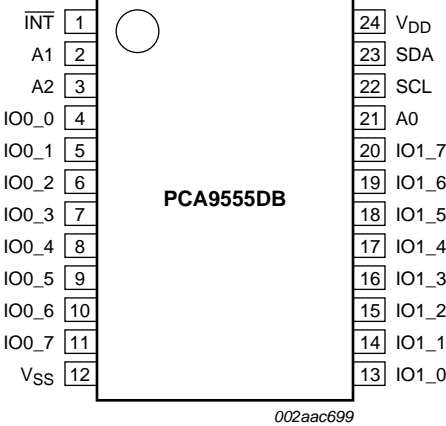


Fig 3. Pin configuration for SSOP24

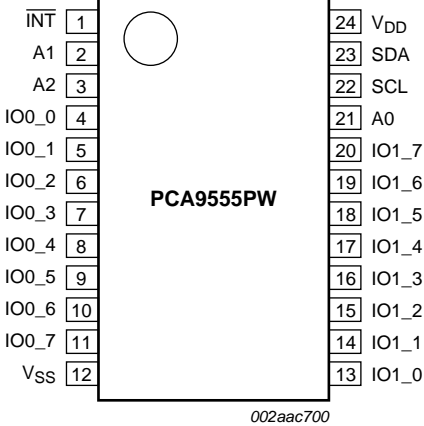


Fig 4. Pin configuration for TSSOP24

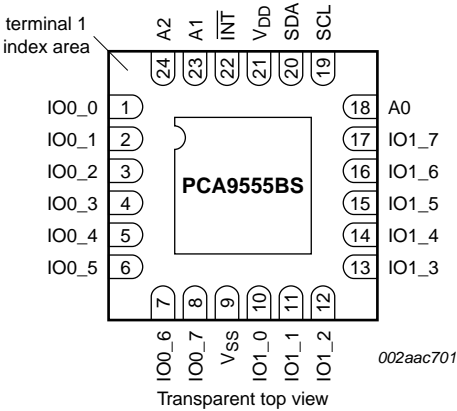


Fig 5. Pin configuration for HVQFN24

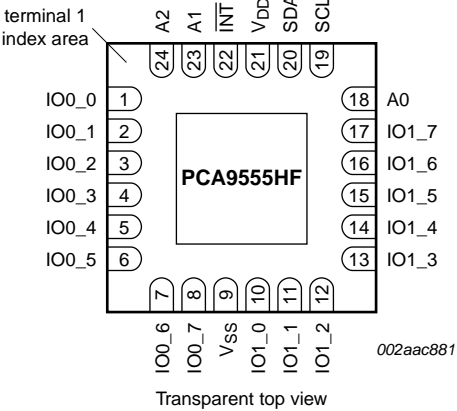


Fig 6. Pin configuration for HWQFN24

## 5.2 Pin description

Table 3. Pin description

| Symbol                  | Pin                      |                     | Description                   |
|-------------------------|--------------------------|---------------------|-------------------------------|
|                         | SO24, SSOP24,<br>TSSOP24 | HVQFN24,<br>HWQFN24 |                               |
| $\overline{\text{INT}}$ | 1                        | 22                  | interrupt output (open-drain) |
| A1                      | 2                        | 23                  | address input 1               |
| A2                      | 3                        | 24                  | address input 2               |
| IO0_0                   | 4                        | 1                   | port 0 input/output           |
| IO0_1                   | 5                        | 2                   |                               |
| IO0_2                   | 6                        | 3                   |                               |
| IO0_3                   | 7                        | 4                   |                               |
| IO0_4                   | 8                        | 5                   |                               |
| IO0_5                   | 9                        | 6                   |                               |
| IO0_6                   | 10                       | 7                   |                               |
| IO0_7                   | 11                       | 8                   |                               |
| V <sub>SS</sub>         | 12                       | 9[1]                | supply ground                 |
| IO1_0                   | 13                       | 10                  | port 1 input/output           |
| IO1_1                   | 14                       | 11                  |                               |
| IO1_2                   | 15                       | 12                  |                               |
| IO1_3                   | 16                       | 13                  |                               |
| IO1_4                   | 17                       | 14                  |                               |
| IO1_5                   | 18                       | 15                  |                               |
| IO1_6                   | 19                       | 16                  |                               |
| IO1_7                   | 20                       | 17                  |                               |
| A0                      | 21                       | 18                  | address input 0               |
| SCL                     | 22                       | 19                  | serial clock line             |
| SDA                     | 23                       | 20                  | serial data line              |
| V <sub>DD</sub>         | 24                       | 21                  | supply voltage                |

- [1] HVQFN and HWQFN package die supply ground is connected to both the V<sub>SS</sub> pin and the exposed center pad. The V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

## 6. Functional description

Refer to [Figure 1 “Block diagram of PCA9555”](#).

### 6.1 Device address

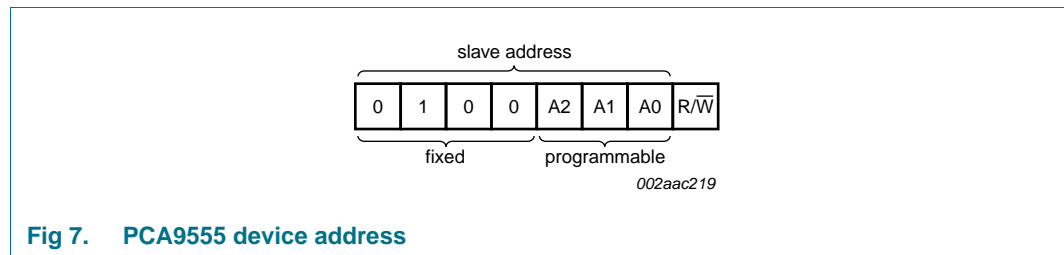


Fig 7. PCA9555 device address

### 6.2 Registers

#### 6.2.1 Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 4. Command byte

| Command | Register                  |
|---------|---------------------------|
| 0       | Input port 0              |
| 1       | Input port 1              |
| 2       | Output port 0             |
| 3       | Output port 1             |
| 4       | Polarity Inversion port 0 |
| 5       | Polarity Inversion port 1 |
| 6       | Configuration port 0      |
| 7       | Configuration port 1      |

### 6.2.2 Registers 0 and 1: Input port registers

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

**Table 5. Input port 0 Register**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | I0.7 | I0.6 | I0.5 | I0.4 | I0.3 | I0.2 | I0.1 | I0.0 |
| Default | X    | X    | X    | X    | X    | X    | X    | X    |

**Table 6. Input port 1 register**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | I1.7 | I1.6 | I1.5 | I1.4 | I1.3 | I1.2 | I1.1 | I1.0 |
| Default | X    | X    | X    | X    | X    | X    | X    | X    |

### 6.2.3 Registers 2 and 3: Output port registers

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

**Table 7. Output port 0 register**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | O0.7 | O0.6 | O0.5 | O0.4 | O0.3 | O0.2 | O0.1 | O0.0 |
| Default | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |

**Table 8. Output port 1 register**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | O1.7 | O1.6 | O1.5 | O1.4 | O1.3 | O1.2 | O1.1 | O1.0 |
| Default | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |

### 6.2.4 Registers 4 and 5: Polarity Inversion registers

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

**Table 9. Polarity Inversion port 0 register**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | N0.7 | N0.6 | N0.5 | N0.4 | N0.3 | N0.2 | N0.1 | N0.0 |
| Default | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**Table 10. Polarity Inversion port 1 register**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | N1.7 | N1.6 | N1.5 | N1.4 | N1.3 | N1.2 | N1.1 | N1.0 |
| Default | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

### 6.2.5 Registers 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high value resistor tied to  $V_{DD}$  at each pin. At reset, the device's ports are inputs with a pull-up to  $V_{DD}$ .

**Table 11. Configuration port 0 register**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | C0.7 | C0.6 | C0.5 | C0.4 | C0.3 | C0.2 | C0.1 | C0.0 |
| Default | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |

**Table 12. Configuration port 1 register**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | C1.7 | C1.6 | C1.5 | C1.4 | C1.3 | C1.2 | C1.1 | C1.0 |
| Default | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |

### 6.3 Power-on reset

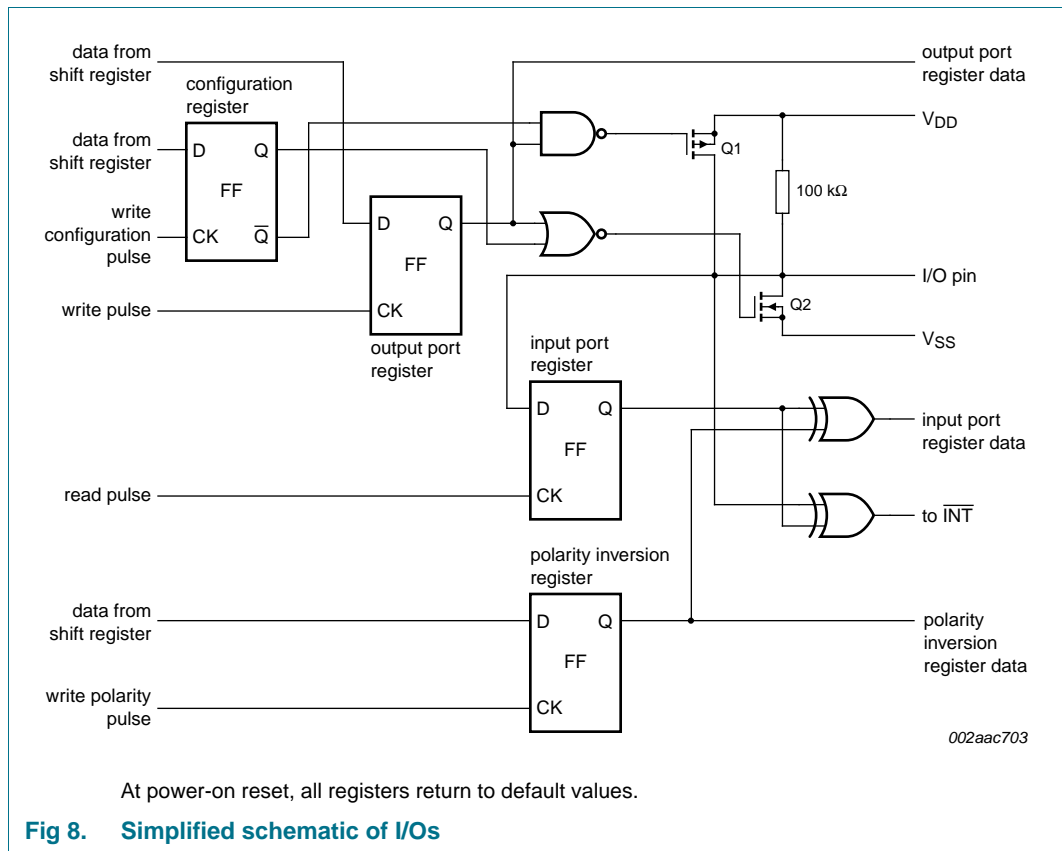
When power is applied to  $V_{DD}$ , an internal power-on reset holds the PCA9555 in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At that point, the reset condition is released and the PCA9555 registers and SMBus state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above  $V_{POR}$ . However, when it is required to reset the part by lowering the power supply, it is necessary to lower it below 0.2 V.

### 6.4 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up to  $V_{DD}$ . The input voltage may be raised above  $V_{DD}$  to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either  $V_{DD}$  or  $V_{SS}$ .





## 6.5 Bus transactions

### 6.5.1 Writing to the port registers

Data is transmitted to the PCA9555 by sending the device address and setting the least significant bit to a logic 0 (see [Figure 7 "PCA9555 device address"](#)). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the PCA9555 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see [Figure 9](#) and [Figure 10](#)). For example, if the first byte is sent to Output Port 1 (register 3), then the next byte will be stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

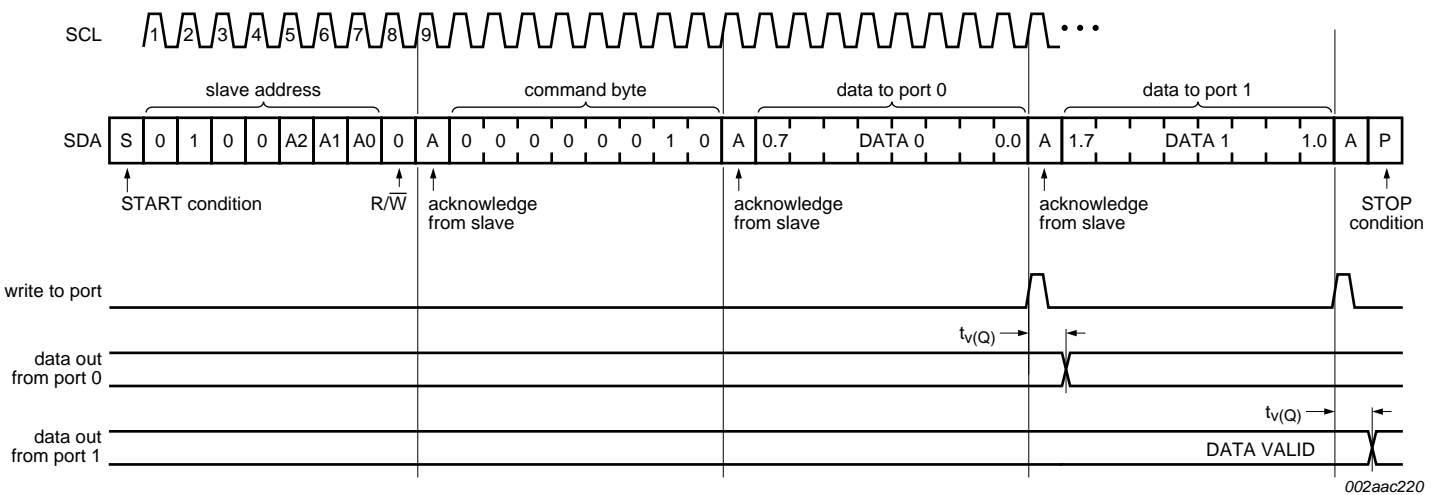


Fig 9. Write to Output port registers

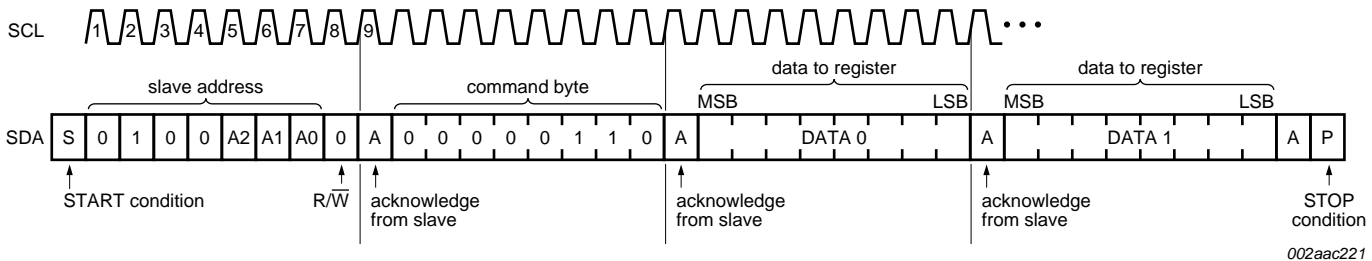
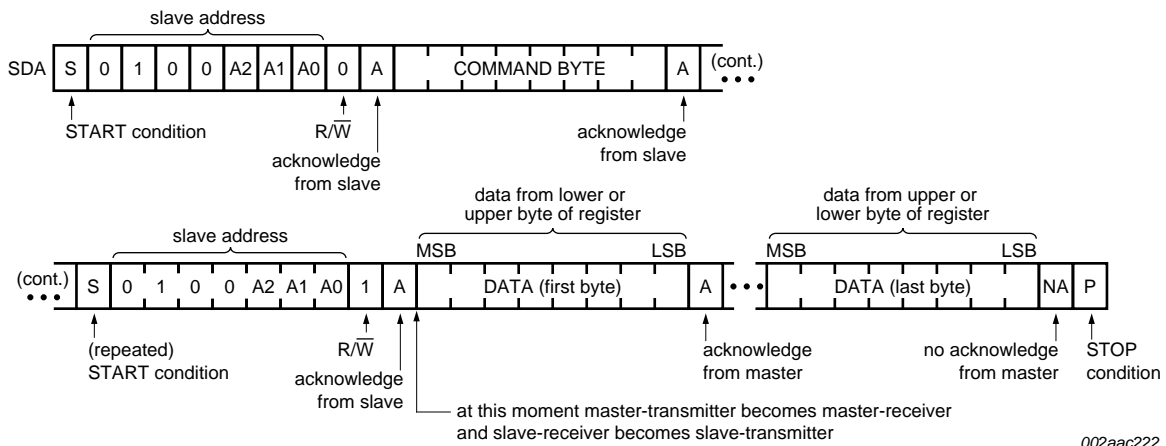


Fig 10. Write to Configuration registers

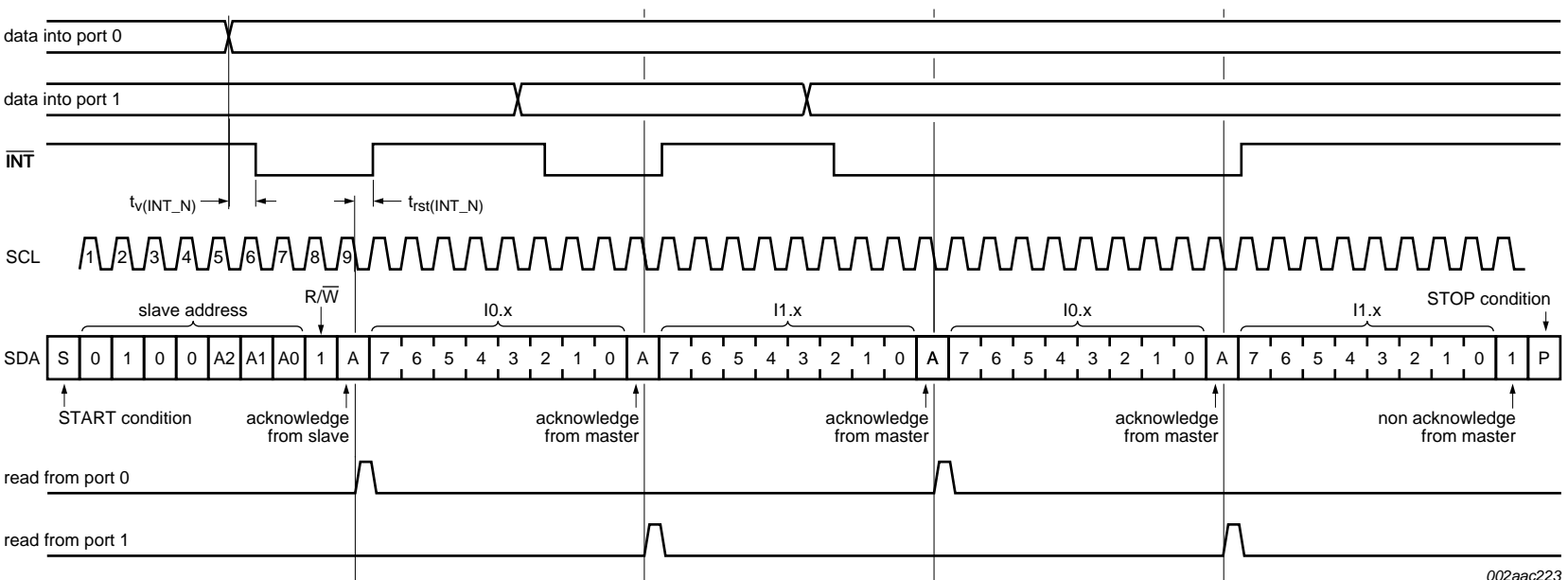
### 6.5.2 Reading the port registers

In order to read data from the PCA9555, the bus master must first send the PCA9555 address with the least significant bit set to a logic 0 (see [Figure 7 “PCA9555 device address”](#)). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PCA9555 (see [Figure 11](#), [Figure 12](#) and [Figure 13](#)). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.



**Remark:** Transfer can be stopped at any time by a STOP condition.

**Fig 11. Read from register**



002aac223

**Remark:** Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Fig 12. Read Input port register, scenario 1



### 6.5.3 Interrupt output

The open-drain interrupt output is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read (see [Figure 12](#)). A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

**Remark:** Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

## 7. Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 14](#)).

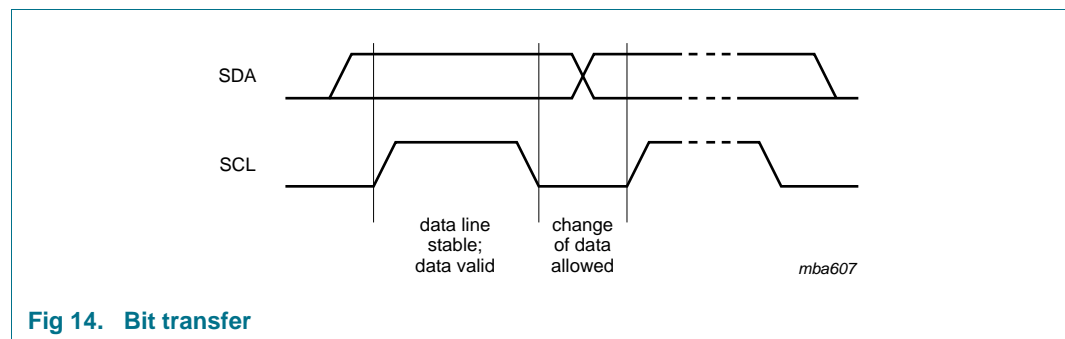


Fig 14. Bit transfer

#### 7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 15](#)).

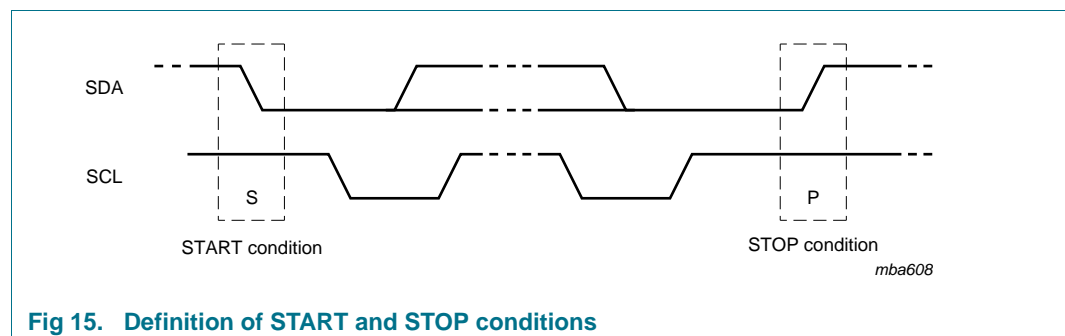


Fig 15. Definition of START and STOP conditions

## 7.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 16](#)).

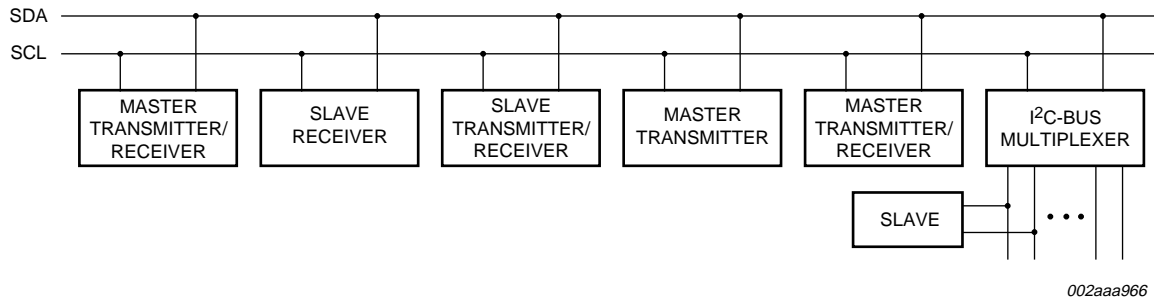


Fig 16. System configuration

## 7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

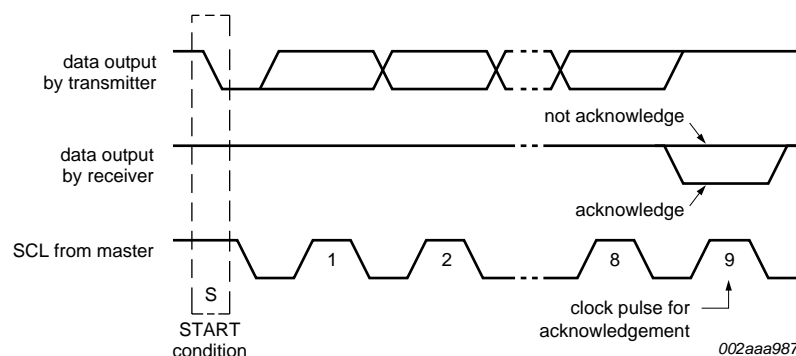
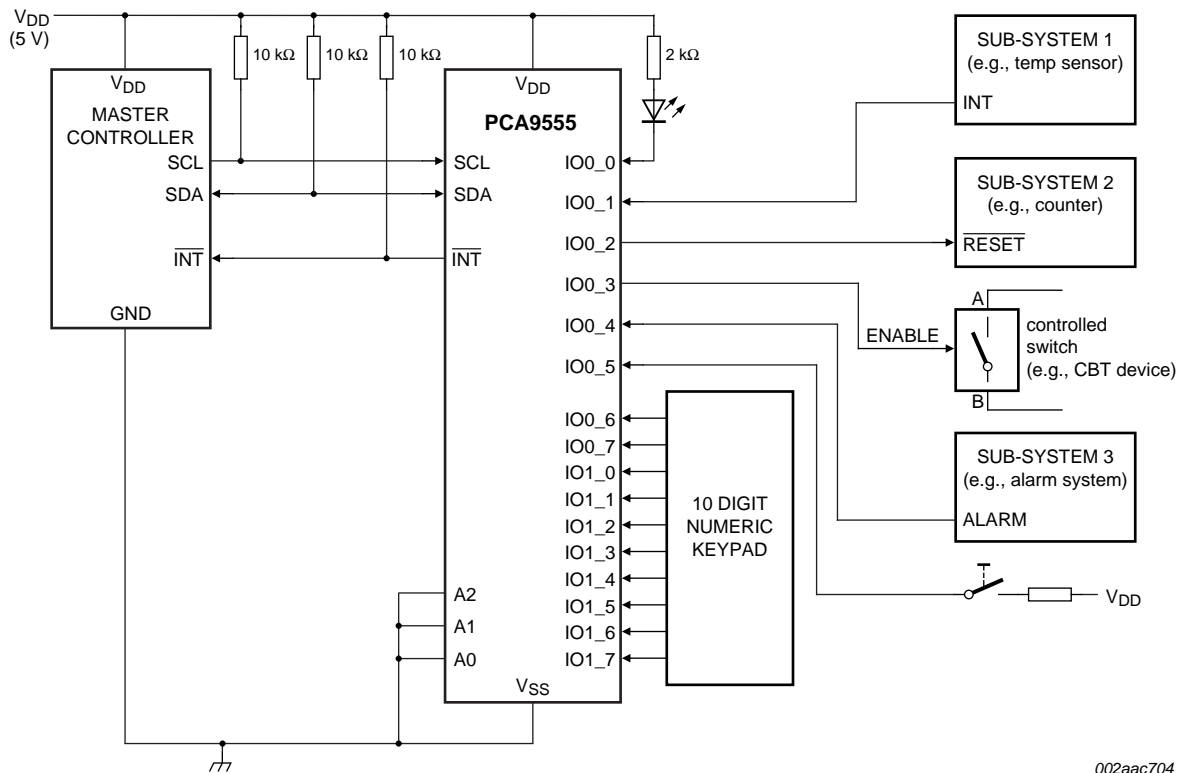


Fig 17. Acknowledgement on the I<sup>2</sup>C-bus

## 8. Application design-in information



002aac704

Device address configured as 0100 000xb for this example.

IO0\_0, IO0\_2, IO0\_3 configured as outputs.

IO0\_1, IO0\_4, IO0\_5 configured as inputs.

IO0\_6, IO0\_7, and IO1\_0 to IO1\_7 configured as inputs.

**Fig 18. Typical application**



## 9. Limiting values

**Table 13. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol              | Parameter                      | Conditions    | Min                   | Max  | Unit |
|---------------------|--------------------------------|---------------|-----------------------|------|------|
| V <sub>DD</sub>     | supply voltage                 |               | −0.5                  | +6.0 | V    |
| V <sub>I/O</sub>    | voltage on an input/output pin |               | V <sub>SS</sub> − 0.5 | 6    | V    |
| I <sub>O</sub>      | output current                 | on an I/O pin | -                     | ±50  | mA   |
| I <sub>I</sub>      | input current                  |               | -                     | ±20  | mA   |
| I <sub>DD</sub>     | supply current                 |               | -                     | 160  | mA   |
| I <sub>SS</sub>     | ground supply current          |               | -                     | 200  | mA   |
| P <sub>tot</sub>    | total power dissipation        |               | -                     | 200  | mW   |
| T <sub>stg</sub>    | storage temperature            |               | −65                   | +150 | °C   |
| T <sub>amb</sub>    | ambient temperature            | operating     | −40                   | +85  | °C   |
| T <sub>j(max)</sub> | maximum junction temperature   |               | -                     | 125  | °C   |

## 10. Static characteristics

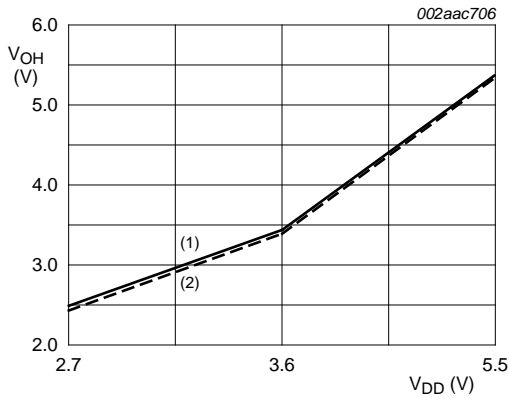
**Table 14. Static characteristics**

$V_{DD} = 2.3 \text{ V to } 5.5 \text{ V}$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                             | Parameter                             | Conditions  | Min                | Typ        | Max           | Unit          |
|------------------------------------|---------------------------------------|---|--------------------|------------|---------------|---------------|
| <b>Supplies</b>                    |                                       |   |                    |            |               |               |
| $V_{DD}$                           | supply voltage                        |   | 2.3                | -          | 5.5           | V             |
| $I_{DD}$                           | supply current                        | Operating mode; $V_{DD} = 5.5 \text{ V}$ ; no load; $f_{SCL} = 100 \text{ kHz}$                             | -                  | 135        | 200           | $\mu\text{A}$ |
| $I_{stb}$                          | standby current                       | Standby mode; $V_{DD} = 5.5 \text{ V}$ ; no load; $V_I = V_{SS}$ ; $f_{SCL} = 0 \text{ kHz}$ ; I/O = inputs | -                  | 1.1        | 1.5           | mA            |
|                                    |                                       | Standby mode; $V_{DD} = 5.5 \text{ V}$ ; no load; $V_I = V_{DD}$ ; $f_{SCL} = 0 \text{ kHz}$ ; I/O = inputs | -                  | 0.25       | 1             | $\mu\text{A}$ |
| $V_{POR}$                          | power-on reset voltage <sup>[1]</sup> | no load; $V_I = V_{DD}$ or $V_{SS}$   | -                  | 1.7        | 2.2           | V             |
| <b>Input SCL; input/output SDA</b> |                                       |   |                    |            |               |               |
| $V_{IL}$                           | LOW-level input voltage               |   | -0.5               | -          | +0.3 $V_{DD}$ | V             |
| $V_{IH}$                           | HIGH-level input voltage              |   | 0.7 $V_{DD}$       | -          | 5.5           | V             |
| $I_{OL}$                           | LOW-level output current              | $V_{OL} = 0.4 \text{ V}$  | 3                  | -          | -             | mA            |
| $I_L$                              | leakage current                       | $V_I = V_{DD} = V_{SS}$   | -1                 | -          | +1            | $\mu\text{A}$ |
| $C_i$                              | input capacitance                     | $V_I = V_{SS}$  | -                  | 6          | 10            | pF            |
| <b>I/Os</b>                        |                                       |   |                    |            |               |               |
| $V_{IL}$                           | LOW-level input voltage               |   | -0.5               | -          | +0.3 $V_{DD}$ | V             |
| $V_{IH}$                           | HIGH-level input voltage              |   | 0.7 $V_{DD}$       | -          | 5.5           | V             |
| $I_{OL}$                           | LOW-level output current              | $V_{DD} = 2.3 \text{ V to } 5.5 \text{ V}$ ; $V_{OL} = 0.5 \text{ V}$                                       | <sup>[2]</sup> 8   | (8 to 20)  | -             | mA            |
|                                    |                                       | $V_{DD} = 2.3 \text{ V to } 5.5 \text{ V}$ ; $V_{OL} = 0.7 \text{ V}$                                       | <sup>[2]</sup> 10  | (10 to 24) | -             | mA            |
| $V_{OH}$                           | HIGH-level output voltage             | $I_{OH} = -8 \text{ mA}$ ; $V_{DD} = 2.3 \text{ V}$   | <sup>[3]</sup> 1.8 | -          | -             | V             |
|                                    |                                       | $I_{OH} = -10 \text{ mA}$ ; $V_{DD} = 2.3 \text{ V}$  | <sup>[3]</sup> 1.7 | -          | -             | V             |
|                                    |                                       | $I_{OH} = -8 \text{ mA}$ ; $V_{DD} = 3.0 \text{ V}$   | <sup>[3]</sup> 2.6 | -          | -             | V             |
|                                    |                                       | $I_{OH} = -10 \text{ mA}$ ; $V_{DD} = 3.0 \text{ V}$  | <sup>[3]</sup> 2.5 | -          | -             | V             |
|                                    |                                       | $I_{OH} = -8 \text{ mA}$ ; $V_{DD} = 4.75 \text{ V}$  | <sup>[3]</sup> 4.1 | -          | -             | V             |
|                                    |                                       | $I_{OH} = -10 \text{ mA}$ ; $V_{DD} = 4.75 \text{ V}$   | <sup>[3]</sup> 4.0 | -          | -             | V             |
| $I_{LIH}$                          | HIGH-level input leakage current      | $V_{DD} = 5.5 \text{ V}$ ; $V_I = V_{DD}$   | -                  | -          | 1             | $\mu\text{A}$ |
| $I_{LIL}$                          | LOW-level input leakage current       | $V_{DD} = 5.5 \text{ V}$ ; $V_I = V_{SS}$   | -                  | -          | -100          | $\mu\text{A}$ |
| $C_i$                              | input capacitance                     |   | -                  | 3.7        | 5             | pF            |
| $C_o$                              | output capacitance                    |   | -                  | 3.7        | 5             | pF            |
| <b>Interrupt INT</b>               |                                       |   |                    |            |               |               |
| $I_{OL}$                           | LOW-level output current              | $V_{OL} = 0.4 \text{ V}$  | 3                  | -          | -             | mA            |
| <b>Select inputs A0, A1, A2</b>    |                                       |   |                    |            |               |               |
| $V_{IL}$                           | LOW-level input voltage               |   | -0.5               | -          | +0.3 $V_{DD}$ | V             |
| $V_{IH}$                           | HIGH-level input voltage              |   | 0.7 $V_{DD}$       | -          | 5.5           | V             |
| $I_{LI}$                           | input leakage current                 |   | -1                 | -          | +1            | $\mu\text{A}$ |

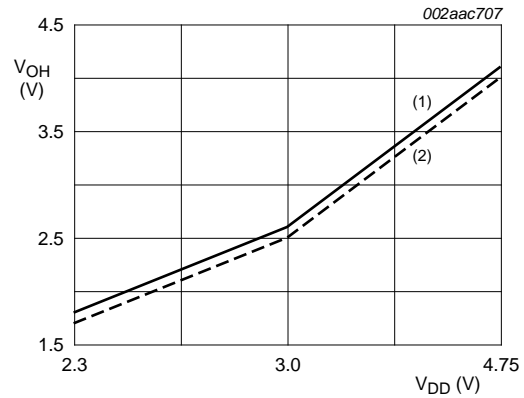
[1]  $V_{DD}$  must be lowered to 0.2 V for at least 5  $\mu\text{s}$  in order to reset part.

- [2] Each I/O must be externally limited to a maximum of 25 mA and each octal (IO0\_0 to IO0\_7 and IO1\_0 to IO1\_7) must be limited to a maximum current of 100 mA for a device total of 200 mA.
- [3] The total current sourced by all I/Os must be limited to 160 mA.



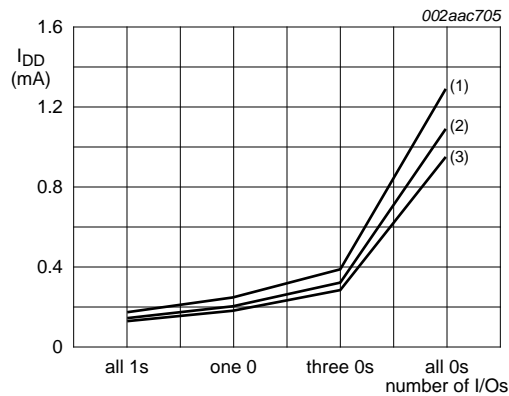
- (1)  $I_{OH} = -8 \text{ mA}$
- (2)  $I_{OH} = -10 \text{ mA}$

Fig 19.  $V_{OH}$  maximum



- (1)  $I_{OH} = -8 \text{ mA}$
- (2)  $I_{OH} = -10 \text{ mA}$

Fig 20.  $V_{OH}$  minimum



$V_{DD} = 5.5 \text{ V}$ ;  $V_{IO} = 5.5 \text{ V}$ ; A2, A1, A0 set to logic 0.

- (1)  $T_{amb} = -40 \text{ °C}$
- (2)  $T_{amb} = +25 \text{ °C}$
- (3)  $T_{amb} = +85 \text{ °C}$

Fig 21.  $I_{DD}$  versus number of I/Os held LOW

## 11. Dynamic characteristics

Table 15. Dynamic characteristics

| Symbol                  | Parameter   | Conditions |     | Standard-mode I <sup>2</sup> C-bus |      | Fast-mode I <sup>2</sup> C-bus |     | Unit |
|-------------------------|---|------------|-----|------------------------------------|------|--------------------------------|-----|------|
|                         |   |            |     | Min                                | Max  | Min                            | Max |      |
| f <sub>SCL</sub>        | SCL clock frequency   |            |     | 0                                  | 100  | 0                              | 400 | kHz  |
| t <sub>BUF</sub>        | bus free time between a STOP and START condition                  |            |     | 4.7                                | -    | 1.3                            | -   | μs   |
| t <sub>HD;STA</sub>     | hold time (repeated) START condition                              |            |     | 4.0                                | -    | 0.6                            | -   | μs   |
| t <sub>SU;STA</sub>     | set-up time for a repeated START condition                        |            |     | 4.7                                | -    | 0.6                            | -   | μs   |
| t <sub>SU;STO</sub>     | set-up time for STOP condition                                    |            |     | 4.0                                | -    | 0.6                            | -   | μs   |
| t <sub>VD;ACK</sub>     | data valid acknowledge time                                       |            | [1] | 0.3                                | 3.45 | 0.1                            | 0.9 | μs   |
| t <sub>HD;DAT</sub>     | data hold time  |            |     | 0                                  | -    | 0                              | -   | ns   |
| t <sub>VD;DAT</sub>     | data valid time   |            | [2] | 300                                | -    | 50                             | -   | ns   |
| t <sub>SU;DAT</sub>     | data set-up time  |            |     | 250                                | -    | 100                            | -   | ns   |
| t <sub>LOW</sub>        | LOW period of the SCL clock                                       |            |     | 4.7                                | -    | 1.3                            | -   | μs   |
| t <sub>HIGH</sub>       | HIGH period of the SCL clock                                      |            |     | 4.0                                | -    | 0.6                            | -   | μs   |
| t <sub>f</sub>          | fall time of both SDA and SCL signals                             |            |     | -                                  | 300  | 20 + 0.1C <sub>b</sub> [3]     | 300 | ns   |
| t <sub>r</sub>          | rise time of both SDA and SCL signals                             |            |     | -                                  | 1000 | 20 + 0.1C <sub>b</sub> [3]     | 300 | ns   |
| t <sub>SP</sub>         | pulse width of spikes that must be suppressed by the input filter |            |     | -                                  | 50   | -                              | 50  | ns   |
| <b>Port timing</b>      |   |            |     |                                    |      |                                |     |      |
| t <sub>V(Q)</sub>       | data output valid time  |            |     | -                                  | 200  | -                              | 200 | ns   |
| t <sub>SU(D)</sub>      | data input set-up time  |            |     | 150                                | -    | 150                            | -   | ns   |
| t <sub>H(D)</sub>       | data input hold time  |            |     | 1                                  | -    | 1                              | -   | μs   |
| <b>Interrupt timing</b> |   |            |     |                                    |      |                                |     |      |
| t <sub>V(INT_N)</sub>   | valid time on pin $\overline{\text{INT}}$                         |            |     | -                                  | 4    | -                              | 4   | μs   |
| t <sub>Rst(INT_N)</sub> | reset time on pin $\overline{\text{INT}}$                         |            |     | -                                  | 4    | -                              | 4   | μs   |

[1] t<sub>VD;ACK</sub> = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] t<sub>VD;DAT</sub> = minimum time for SDA data out to be valid following SCL LOW.

[3] C<sub>b</sub> = total capacitance of one bus line in pF.

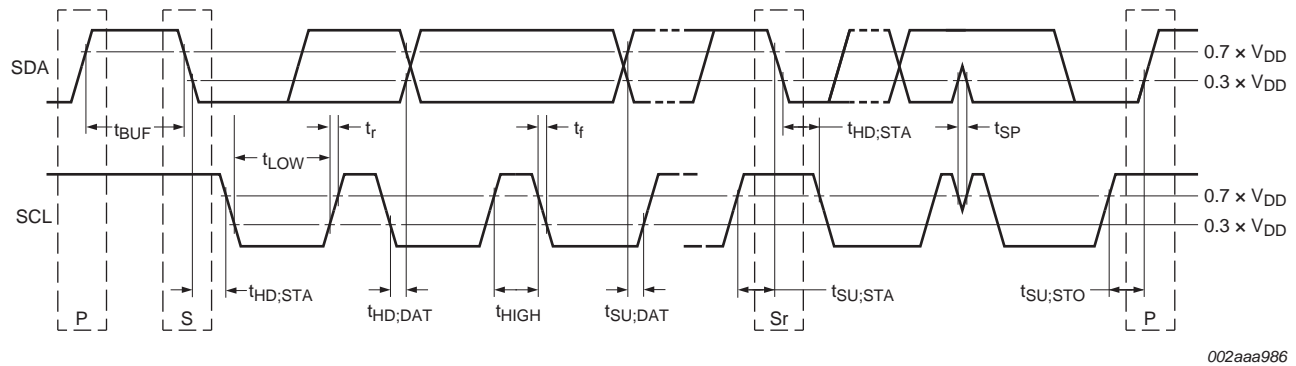
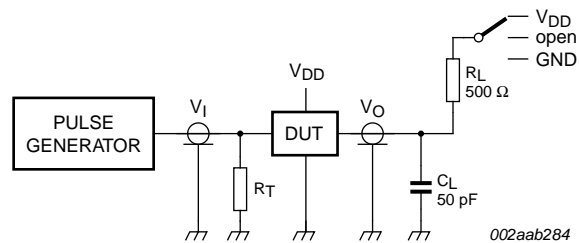


Fig 22. Definition of timing on the I<sup>2</sup>C-bus

## 12. Test information



$R_L$  = load resistor.

$C_L$  = load capacitance includes jig and probe capacitance.

$R_T$  = termination resistance should be equal to the output impedance of  $Z_o$  of the pulse generators.

Fig 23. Test circuitry for switching times

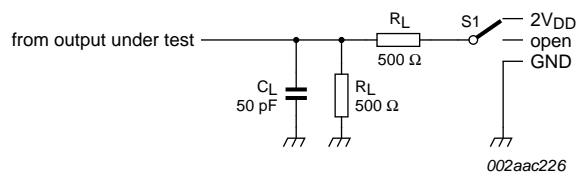


Fig 24. Load circuit

# 13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

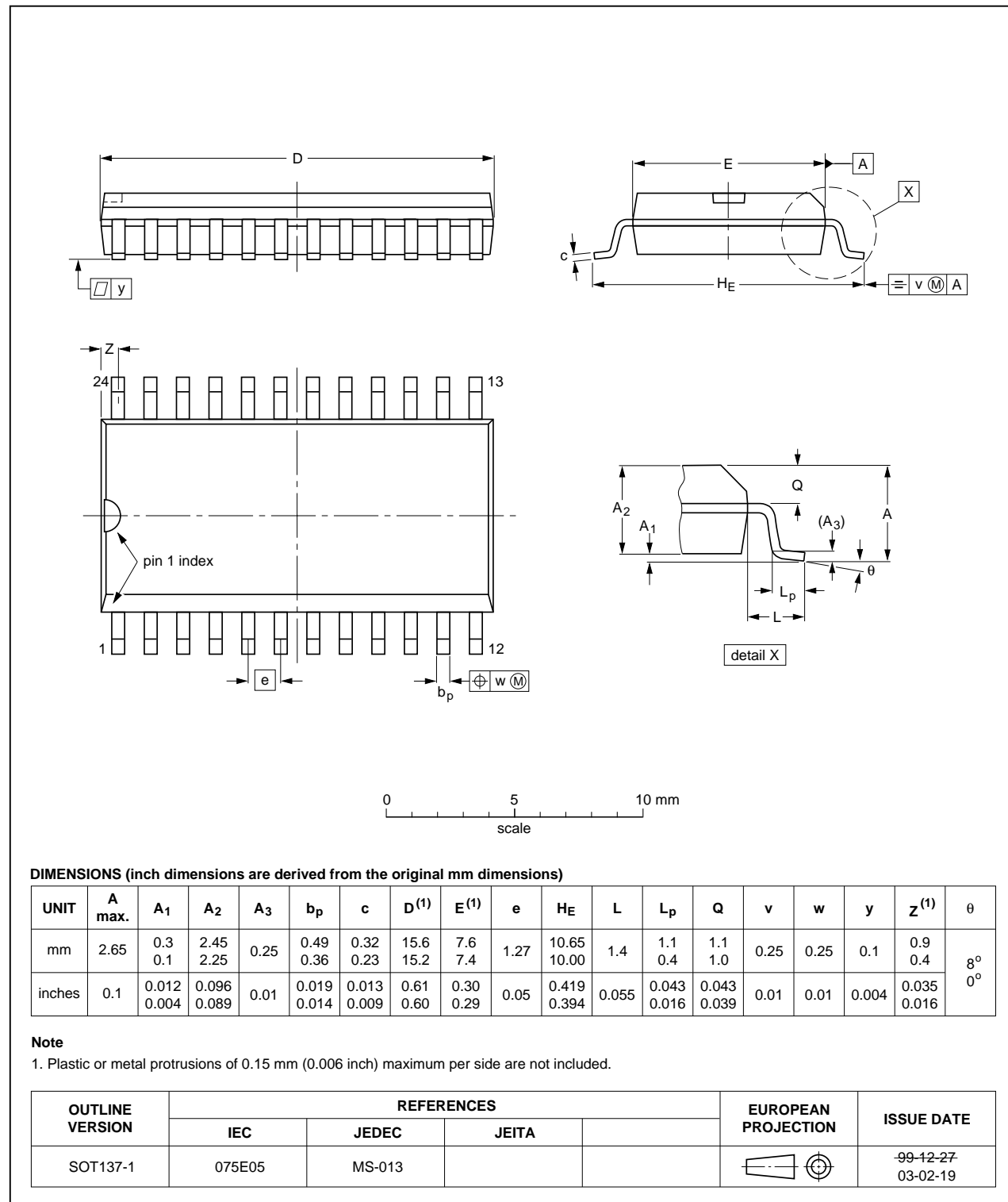


Fig 25. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

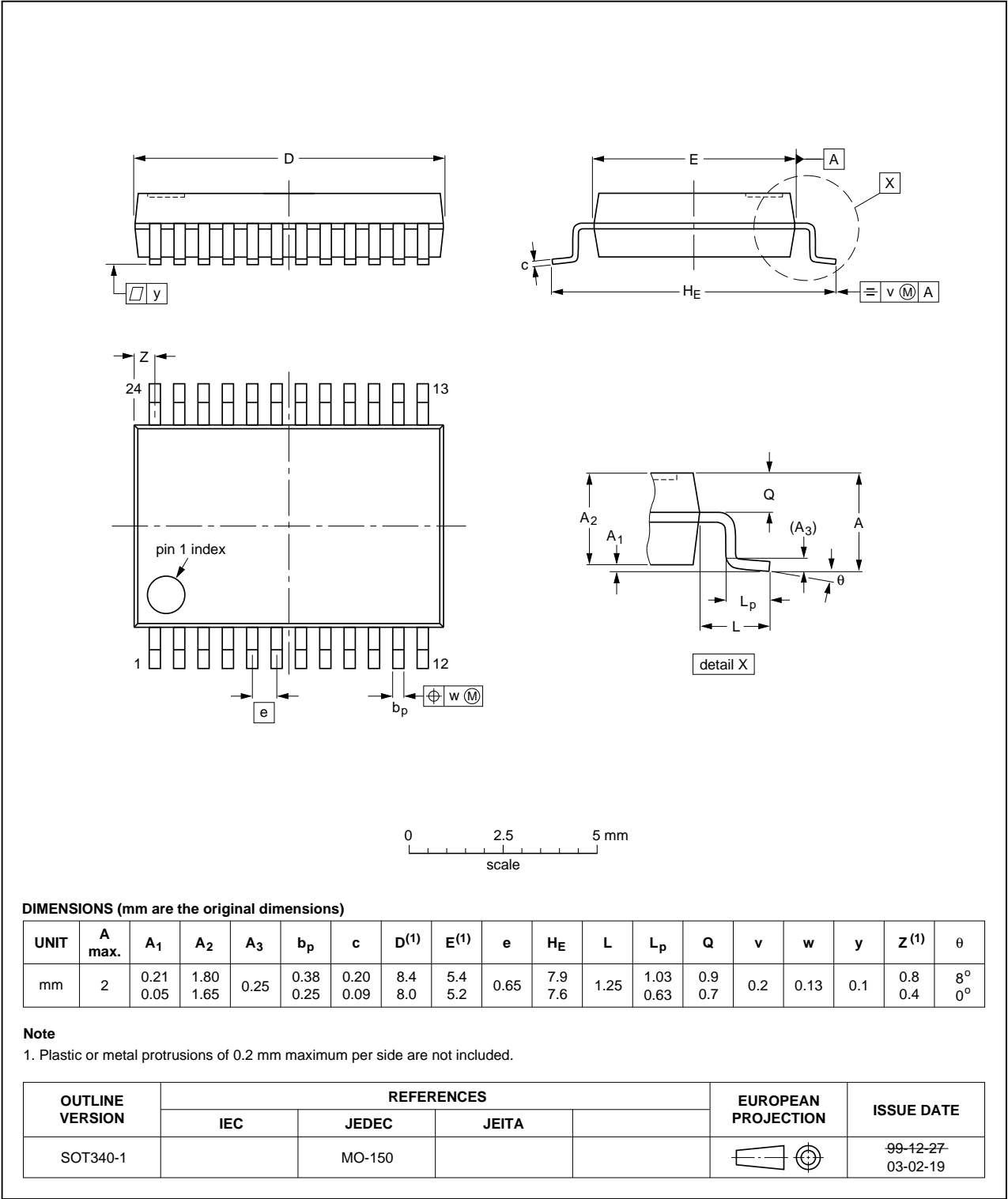


Fig 26. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

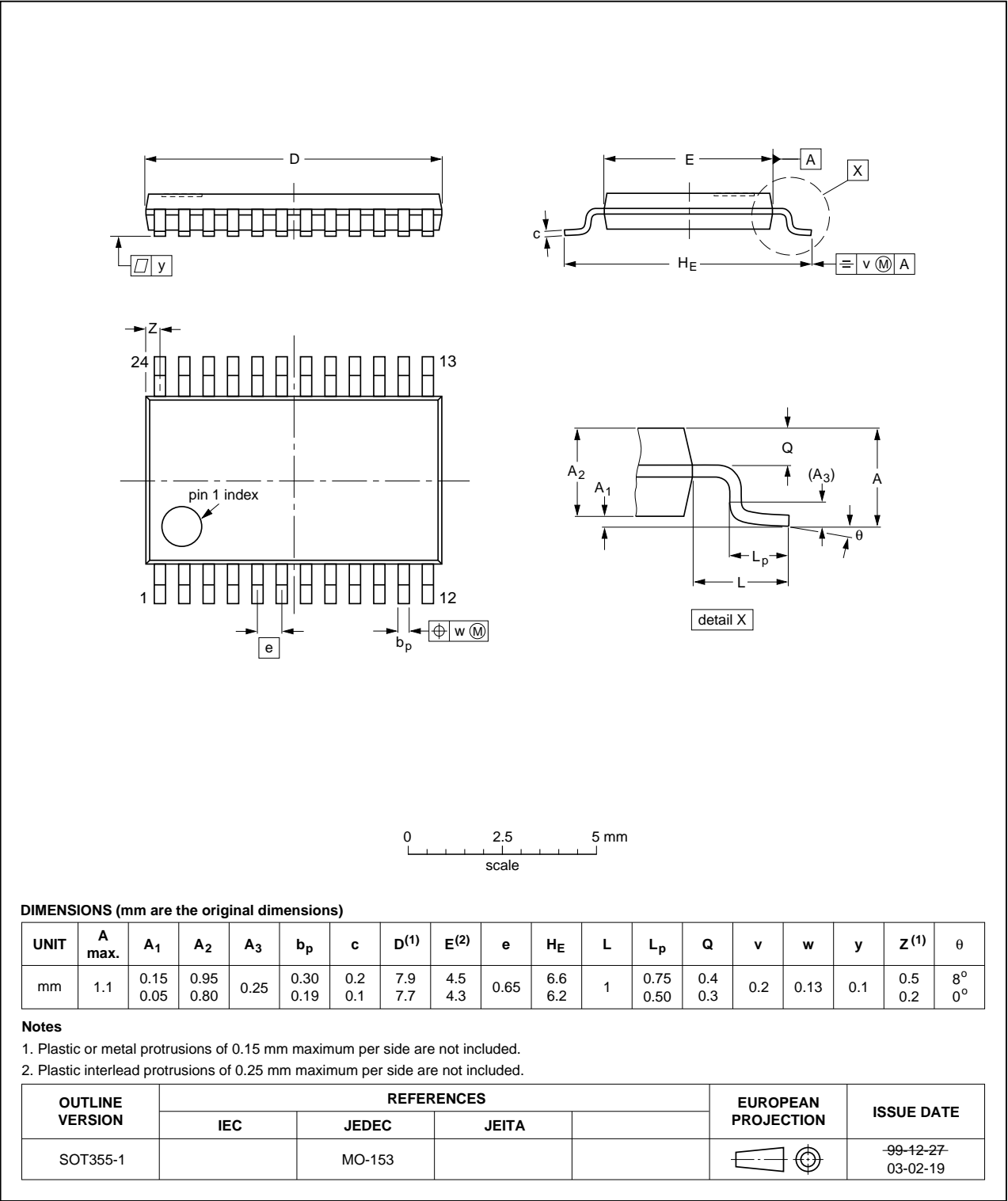
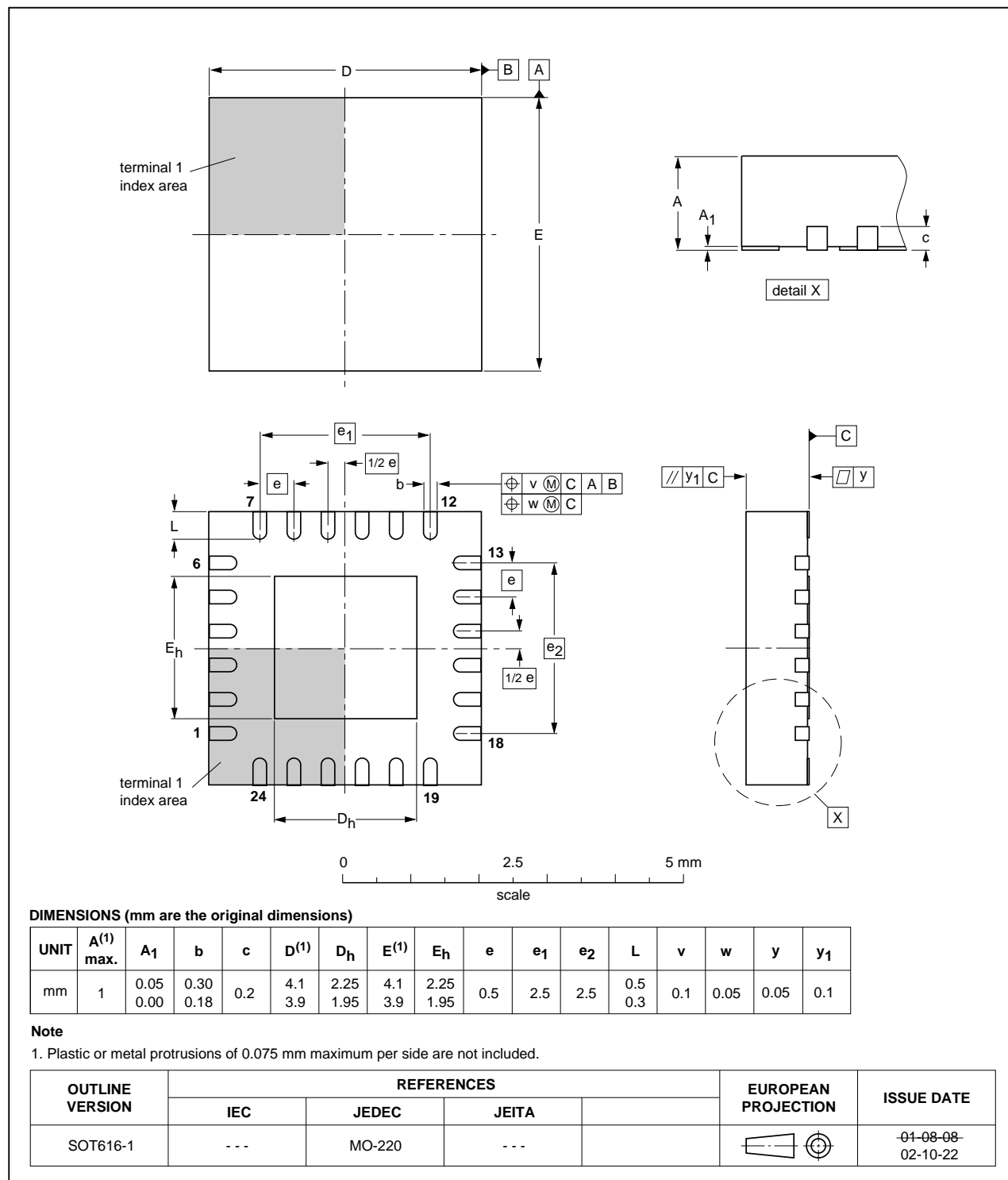


Fig 27. Package outline SOT355-1 (TSSOP24)



**HVQFN24: plastic thermal enhanced very thin quad flat package; no leads;**  
**24 terminals; body 4 x 4 x 0.85 mm**

**SOT616-1**



**Fig 28. Package outline SOT616-1 (HVQFN24)**

HWQFN24: plastic thermal enhanced very very thin quad flat package; no leads;  
24 terminals; body 4 x 4 x 0.75 mm

SOT994-1

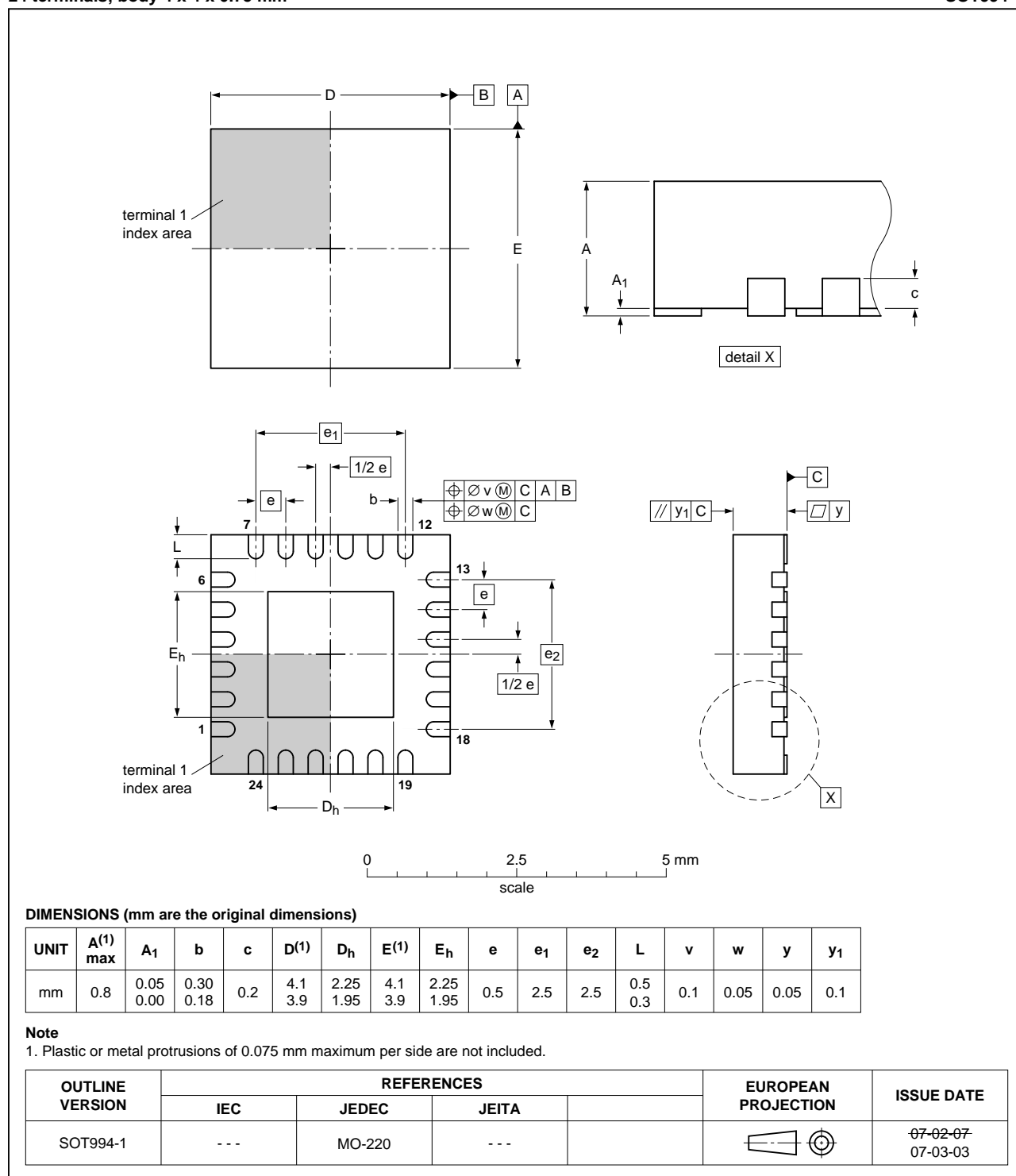


Fig 29. Package outline SOT994-1 (HWQFN24)

## 14. Handling information

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All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

## 15. Soldering of SMD packages

---

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 30](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 16](#) and [17](#)

**Table 16. SnPb eutectic process (from J-STD-020C)**

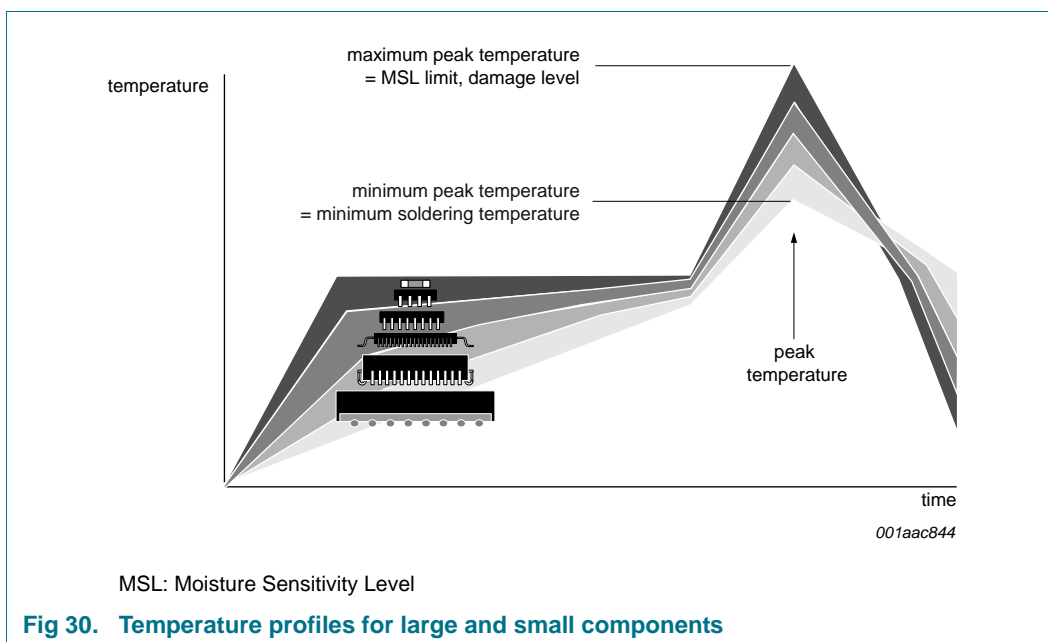
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 17. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 30](#).



For further information on temperature profiles, refer to Application Note *AN10365* "Surface mount reflow soldering description".

## 16. Soldering of through-hole mount packages

### 16.1 Introduction to soldering through-hole mount packages

This text gives a very brief insight into wave, dip and manual soldering.

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

### 16.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg(max)}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### 16.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

## 16.4 Package related soldering information

Table 18. Suitability of through-hole mount IC packages for dipping and wave soldering

| Package                         | Soldering method |                         |
|---------------------------------|------------------|-------------------------|
|                                 | Dipping          | Wave                    |
| CPGA, HCPGA                     | -                | suitable                |
| DBS, DIP, HDIP, RDBS, SDIP, SIL | suitable         | suitable <sup>[1]</sup> |
| PMFP <sup>[2]</sup>             | -                | not suitable            |

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

## 17. Abbreviations

Table 19. Abbreviations

| Acronym              | Description                                |
|----------------------|--|
| CMOS                 | Complementary Metal Oxide Semiconductor    |
| GPIO                 | General Purpose Input/Output               |
| I <sup>2</sup> C-bus | Inter-Integrated Circuit bus               |
| SMBus                | System Management Bus                      |
| I/O                  | Input/Output                               |
| ACPI                 | Advanced Configuration and Power Interface |
| LED                  | Light Emitting Diode                       |
| ESD                  | ElectroStatic Discharge                    |
| HBM                  | Human Body Model                           |
| MM                   | Machine Model                              |
| CDM                  | Charged Device Model                       |
| PCB                  | Printed-Circuit Board                      |
| FET                  | Field-Effect Transistor                    |
| MSB                  | Most Significant Bit                       |
| LSB                  | Least Significant Bit                      |

## 18. Revision history

Table 20. Revision history

| Document ID                   | Release date  | Data sheet status  | Change notice                     | Supersedes |
|-------------------------------|---|--------------------|-----------------------------------|------------|
| PCA9555 v.10                  | 20171108  | Product data sheet | 201710002I                        | PCA9555_9  |
| Modifications:                | <ul style="list-style-type: none"> <li>• <a href="#">Table 14 “Static characteristics”</a>: Corrected V<sub>POR</sub> typ and max limit</li> <li>• Added <a href="#">Section 3.1 “Ordering options”</a></li> <li>• Obsolete part PCA9555N (DIP24, SOT101-1) removed</li> </ul>  |                    |                                   |            |
| PCA9555 v.9                   | 20170510  | Product data sheet | -                                 | PCA9555_8  |
| Modifications:                | <ul style="list-style-type: none"> <li>• <a href="#">Table 13 “Limiting values”</a>, added row for T<sub>j(max)</sub></li> </ul>  |                    |                                   |            |
| PCA9555_8                     | 20091022  | Product data sheet | -                                 | PCA9555_7  |
| Modifications:                | <ul style="list-style-type: none"> <li>• <a href="#">Table 2 “Ordering options”</a>, Topside mark for TSSOP24 package, PCA9555PW, is changed from “PCA9555PW” to “PCA9555”</li> <li>• <a href="#">Figure 12 “Read Input port register, scenario 1”</a> modified</li> <li>• <a href="#">Figure 13 “Read Input port register, scenario 2”</a> modified</li> <li>• <a href="#">Table 14 “Static characteristics”</a>, <a href="#">Table note [1]</a> modified (added phrase “for at least 5 μs”)</li> <li>• updated soldering information</li> </ul> |                    |                                   |            |
| PCA9555_7                     | 20070605  | Product data sheet | -                                 | PCA9555_6  |
| PCA9555_6                     | 20060825  | Product data sheet | -                                 | PCA9555_5  |
| PCA9555_5<br>(9397 750 14125) | 20040930  | Product data sheet | -                                 | PCA9555_4  |
| PCA9555_4<br>(9397 750 13271) | 20040727  | Product data sheet | -                                 | PCA9555_3  |
| PCA9555_3<br>(9397 750 10164) | 20020726  | Product data       | 853-2252 28672 of<br>2002 July 26 | PCA9555_2  |
| PCA9555_2<br>(9397 750 09818) | 20020513  | Product data       | -                                 | PCA9555_1  |
| PCA9555_1<br>(9397 750 08343) | 20010507  | Product data       | -                                 | -          |

## 19. Legal information

### 19.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 20. Contact information

For more information, please visit: <http://www.nxp.com>

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